

# **MSC8156AMC Hardware Design Specification**

The document describes the hardware design of MSC8156AMC.

## **0.1 Change History**

Table 0-1 shows the change history of this document.

**Table 0-1. Change History**

Date	Author	Version	Notes
Feb , 2009		0.1	First Draft

## **0.2 Design Purpose**

MSC8156AMC is designed to serve the following purposes:

- E/// evaluation
- DSP software development for AP customers

## **0.3 Features Specification**

The MSC8156AMC-B is designed with the following features:

- One 8-port x4 sRIO switch which support up to 3.125Gbaud for each lane
- One 6-port SGMII Ethernet switch
- Two x4 sRIO connections to port [4:7] and port [8:11] of back plane
- Two 1000 Base-X connections to port 0 and port 1 of back plane
- One Ethernet Quad PHY for RGMII to SGMII interchange
- One RS232 Connector, RJ45 Connector and reset button on front panel
- Two CPLDs for power sequence, clock, reset, interrupt and misc. logic control
- Switching and LDO power supplies for different voltages including 1V, 1.2V, 1.5V, 2.5V and 3.3V
- Three QSH connectors for six x4 sRIO interfaces, dual x4 sRIO interfaces from each DSP

- Two BSH connectors for RGMII, DSP GPIO, Interrupt, reset, clocks and power supplies
- Single width full height AMC likes form factor
- Support IPMB interface
- Optional Module management controller

## 0.4 Mechanical and Electrical Specification

MSC8156AMC-B will be designed to be

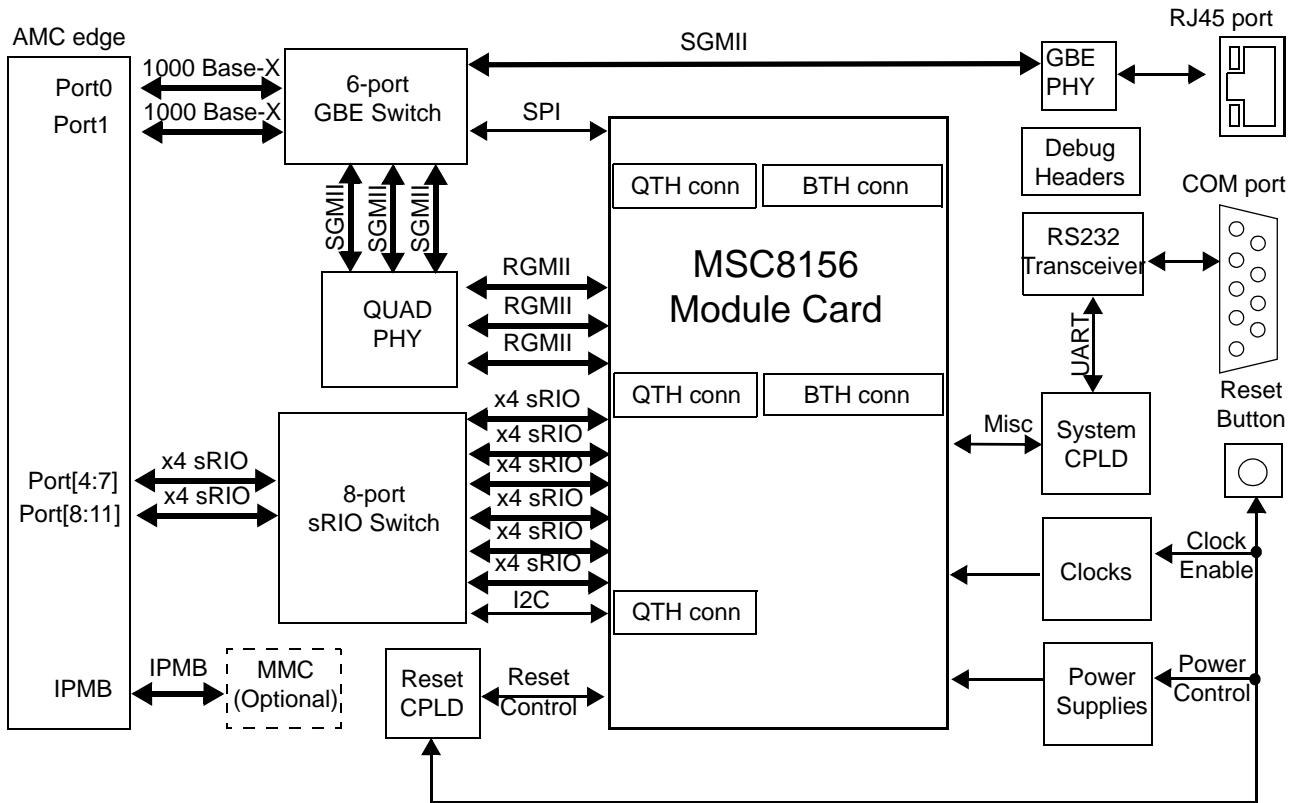
- Single width full height AMC likes form factor
- RoHS compliant

## 0.5 Design Information

Here describes the hardware design details and considerations of different features.

## 0.5.1 Block Diagram

Figure 0-1 shows the system block diagram of MSC8156AMC-B.



**Figure 0-1. MSC8156AMC Base System Block Diagram**

## 0.5.2 Serial RapidIO

8-port x4 sRIO switch will be used. (vendor and part number??)

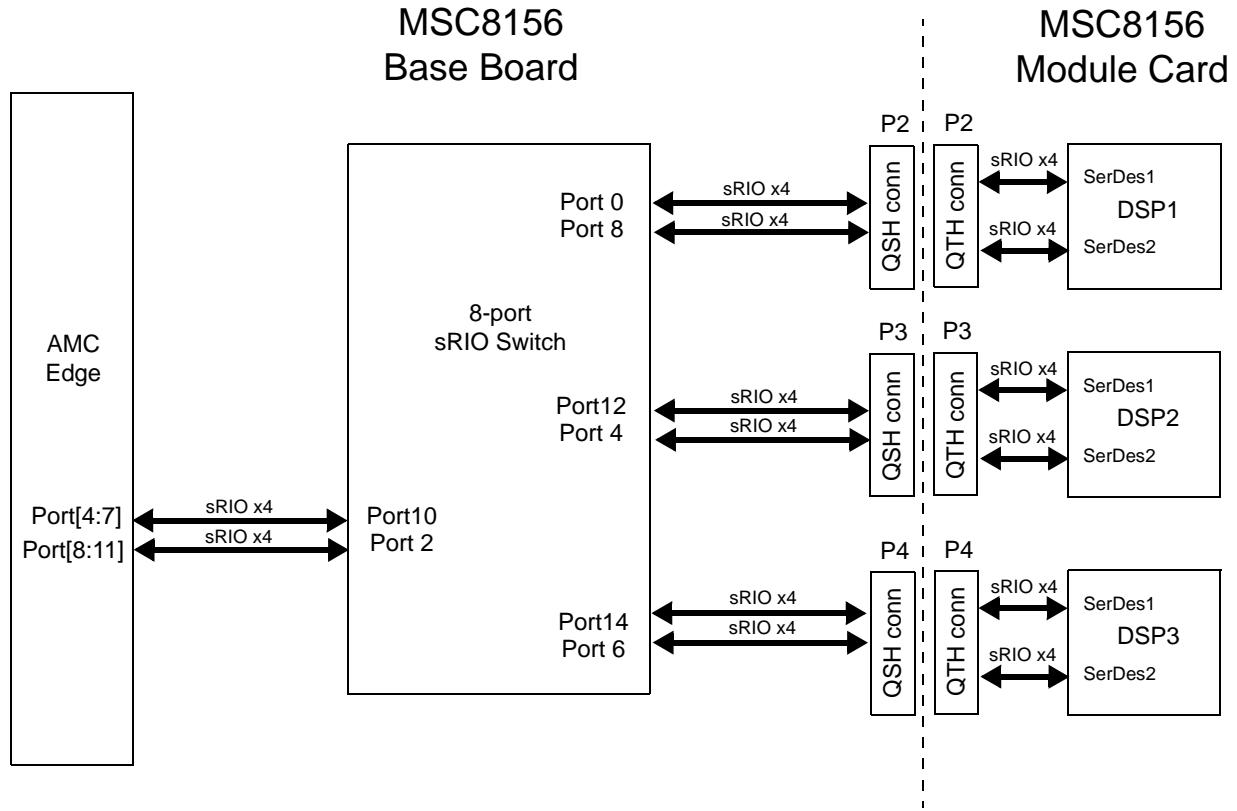
DSP0 will connect two 4x SRIO links to the switch.

DSP1 will connect two 4x SRIO links to the switch.

DSP2 will connect one 4x SRIO link to the switch and one 4x SRIO link to AMC connector (Port 12-15).

Three 4x SRIO links from the switch will connect to AMC connector (Port 04-07, 08-11, 17-20).

Figure 0-3 shows the sRIO connection.



**Figure 0-2. sRIO connection**

### 0.5.3 Gigabit Ethernet Connection

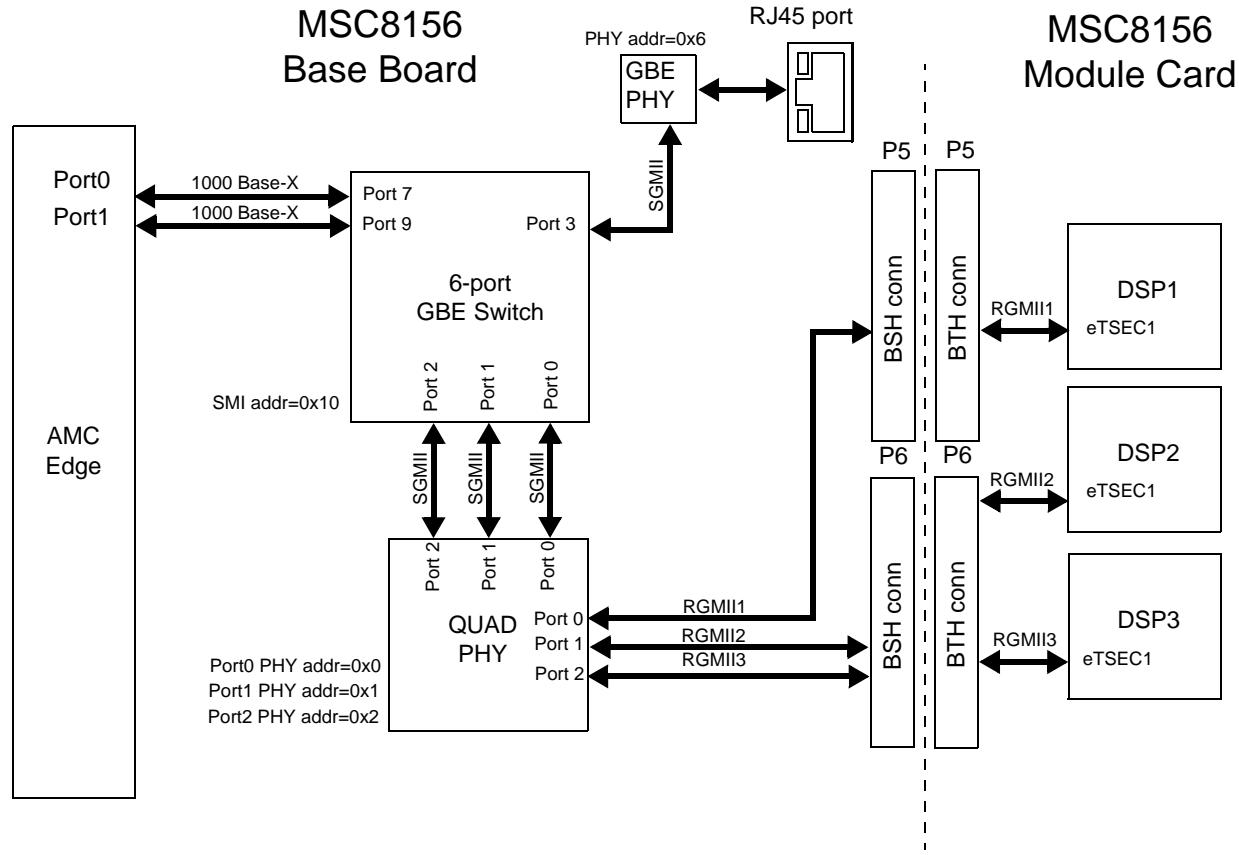
Each DSP should utilize one RGMII port for Ethernet connection.

An Ethernet switch will be used for data routing flexibility. (vendor and part numbers??)

Two Ethernet interfaces (SerDes)will be routed to AMC connector.

One Ethernet interface (copper) will be routed to AMC card front panel.

[Figure 0-3](#) shows the Ethernet connection.



**Figure 0-3. MSC8156AMC Ethernet Connection**

## 0.5.4 Power supplies

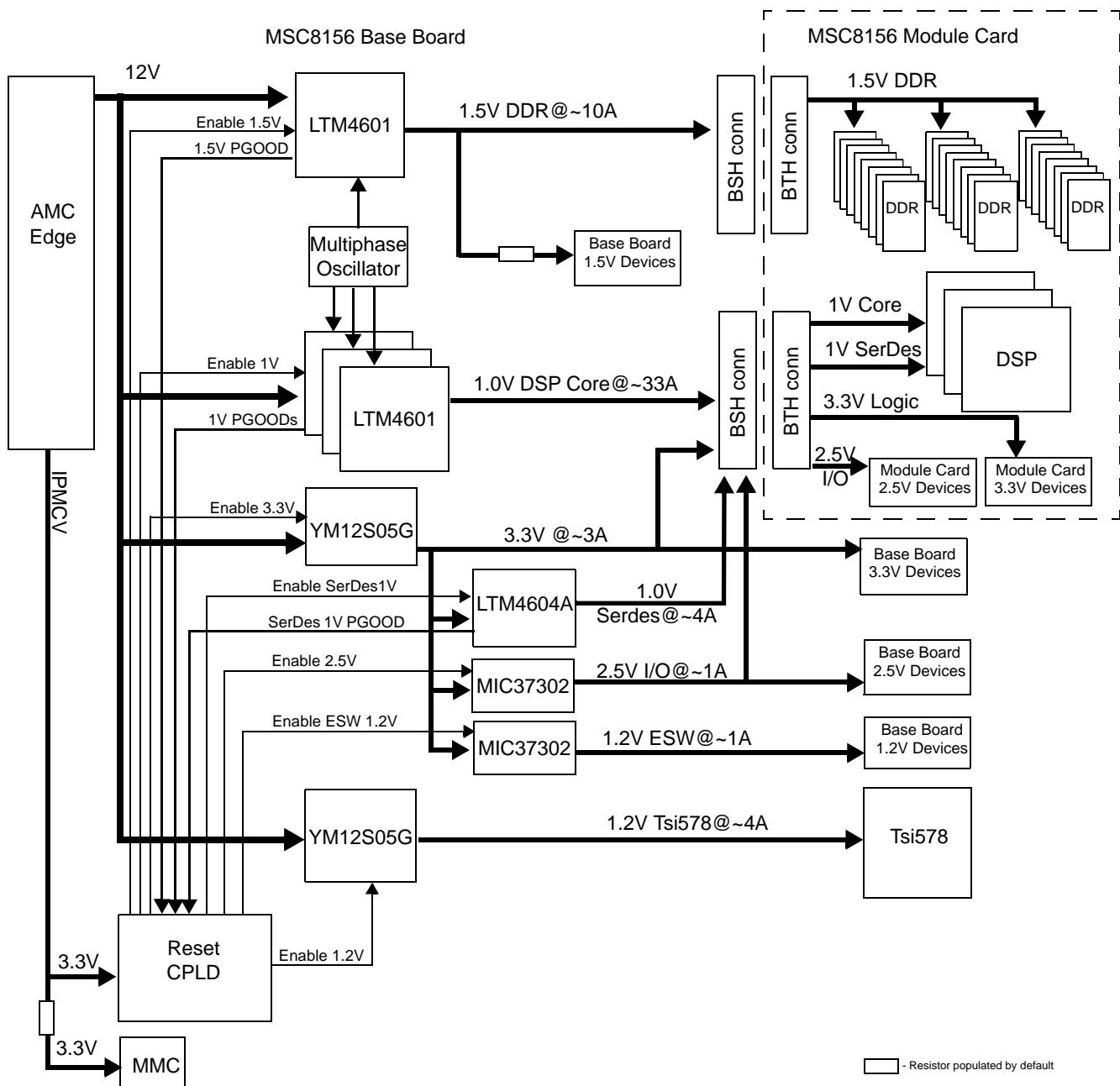


Figure 0-4. MSC8156AMC Power System

## 0.5.5 Clocks

These are the clocks required:

1. System clock, SerDes reference clock and eTSEC clock for DSPs
2. Clocks for QUAD PHY, Ethernet switch and single GBE PHY
3. sRIO clock

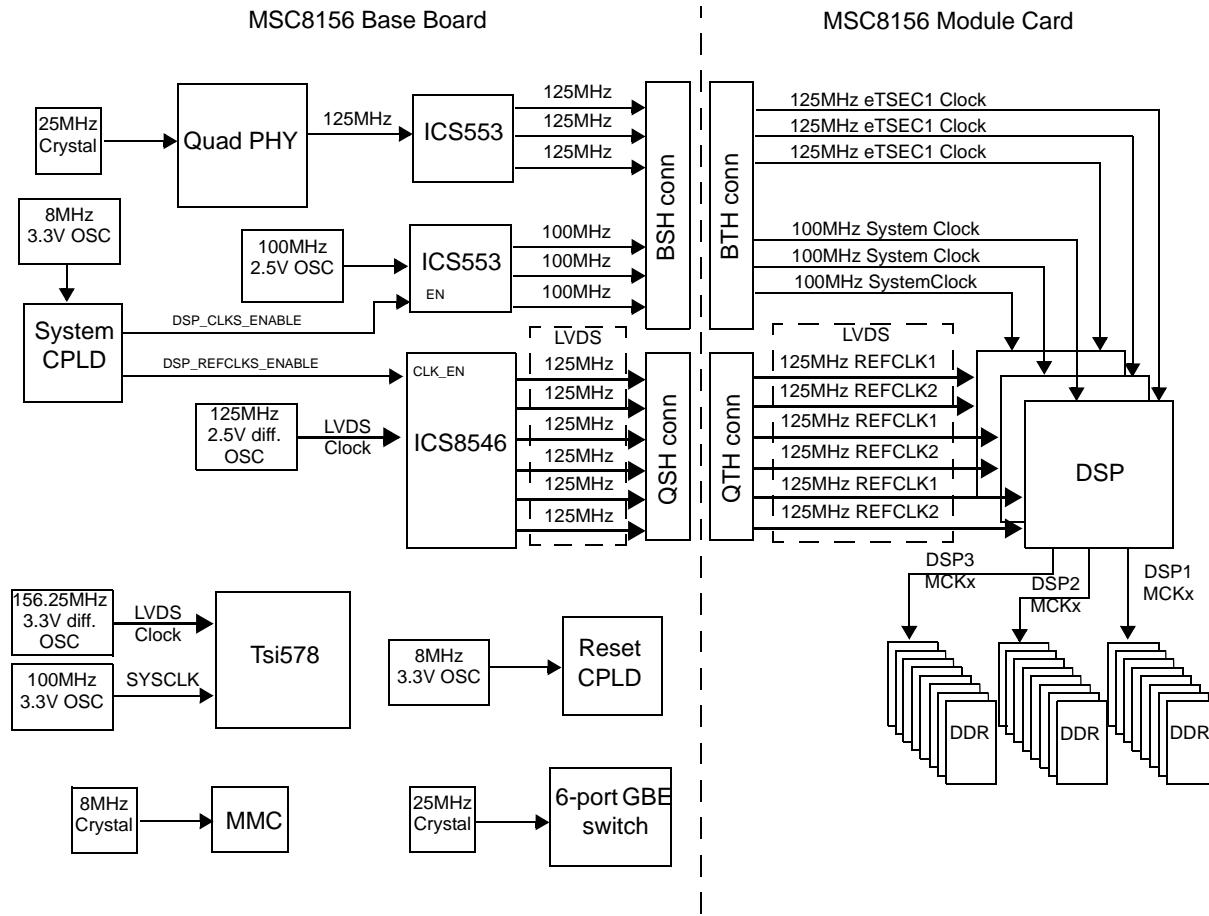
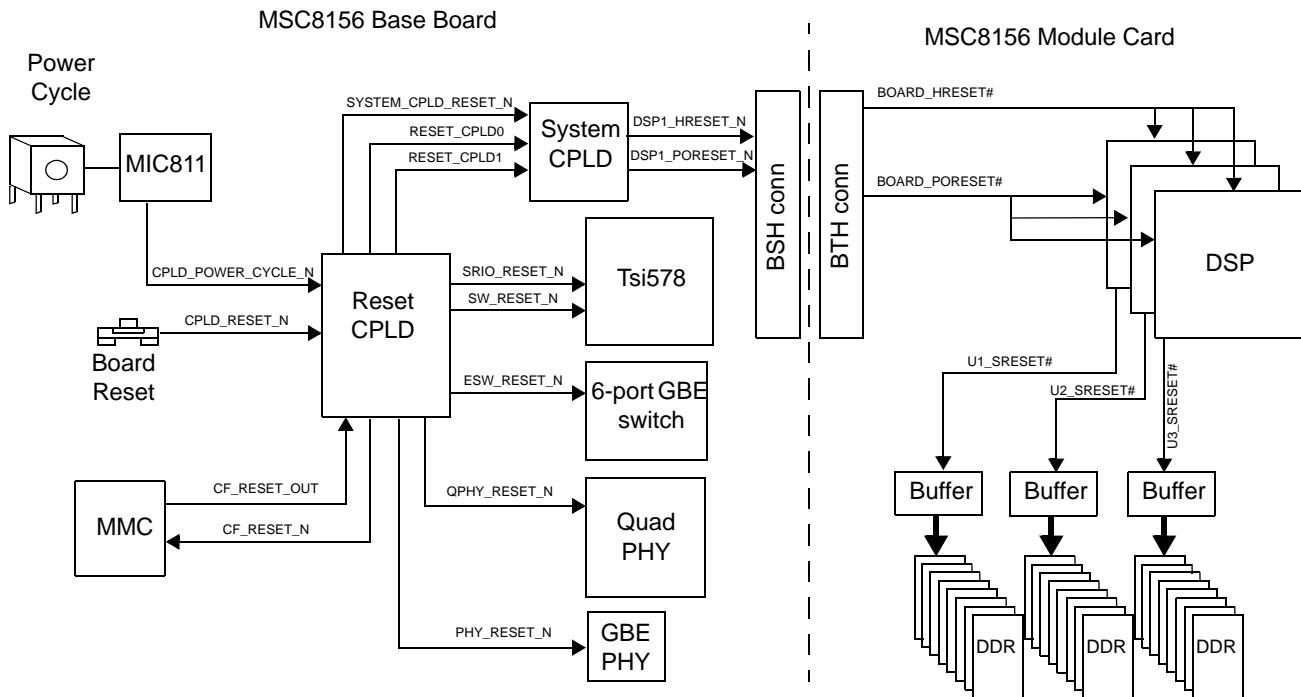
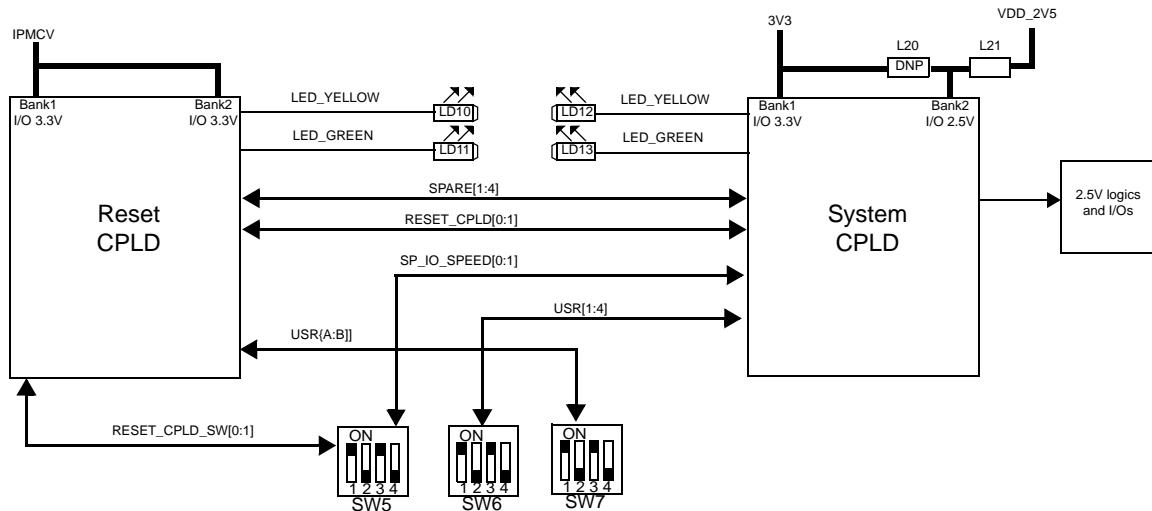


Figure 0-5. Clocks Distribution

## 0.5.6 Reset

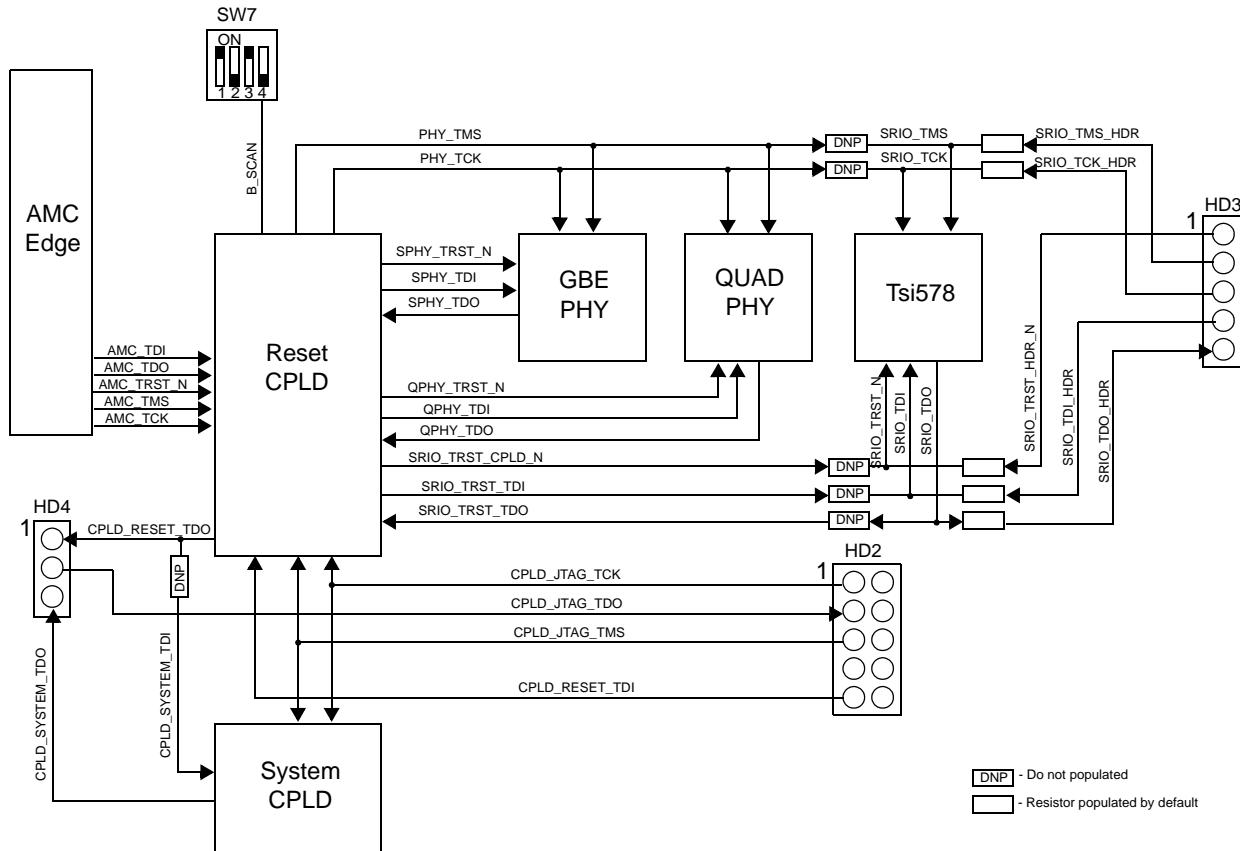


## 0.5.7 CPLDs



Two CPLDs (Altera EPM240T100C5N) are used on MSC8156AMC which are Reset CPLD and System CPLD to control power sequence, clocks enable, reset logic, DSP GPIO connection, interrupt and misc control of the board.

## 0.5.8 JTAG



**Figure 0-6. JTAG Connection of Base Board**

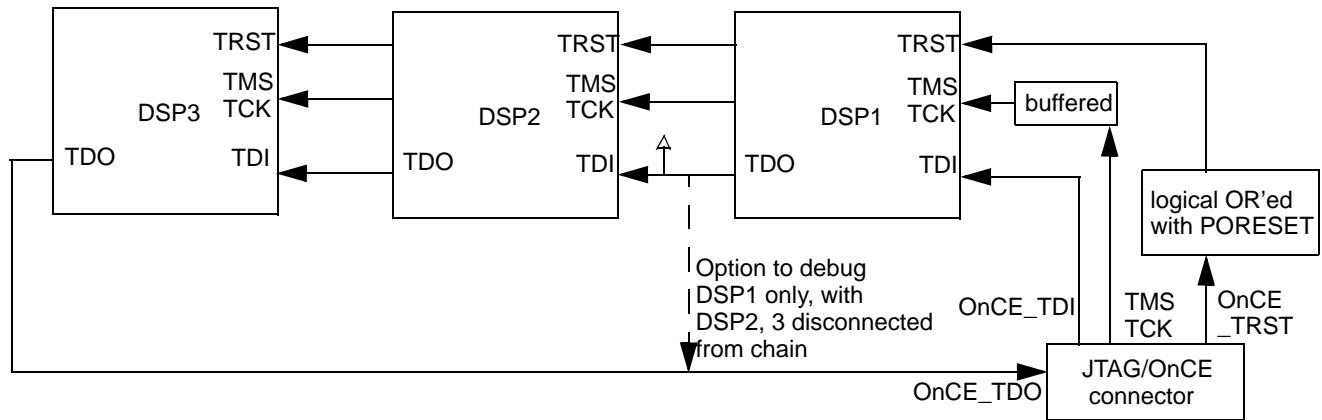
The JTAG/OnCE chains all three DSPs on the module card. Only one JTAG/OnCE connector is used. By resistor option, the JTAG/OnCE port can be isolated such that only the first DSP is connected to the JTAG/OnCE connector.

TRST# is connected to all DSPs. It is a logical OR'ed of OnCE\_TRST# (with pull up) and PORESET#.

TMS is pulled up and buffered, and it is connected to all DSPs.

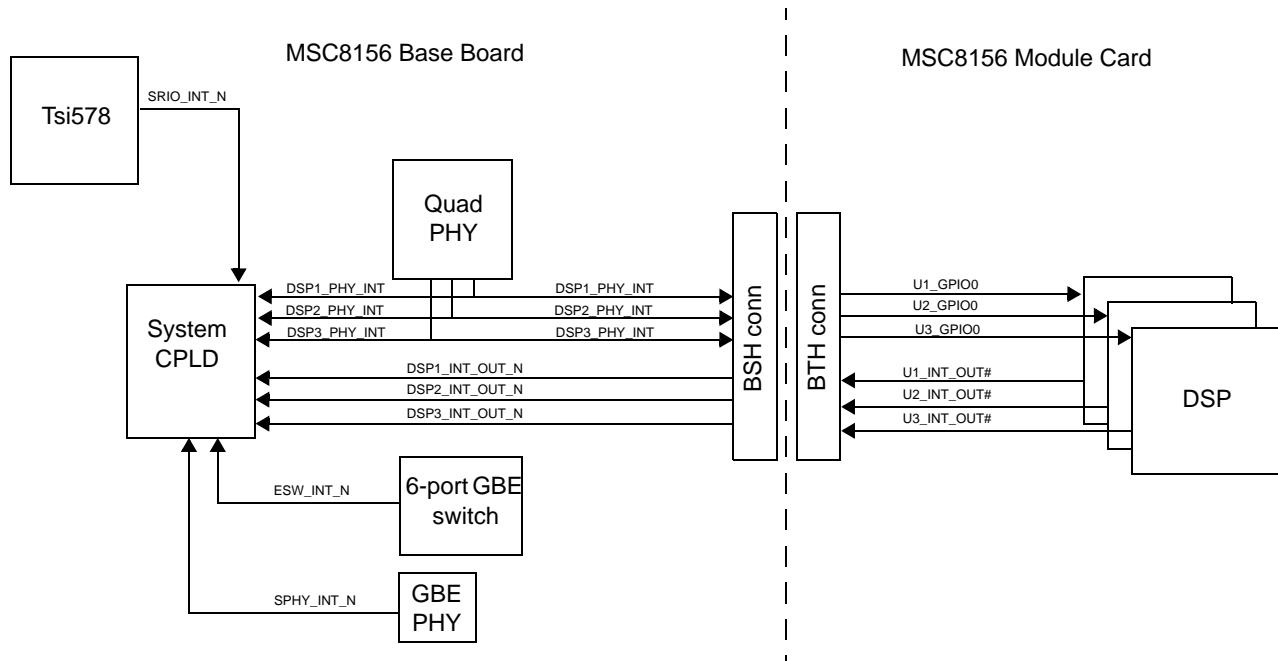
TCK is pulled down and buffered, and it is connected to all DSPs.

Figure 0-7 shows the JTAG/OnCE connection block diagram.

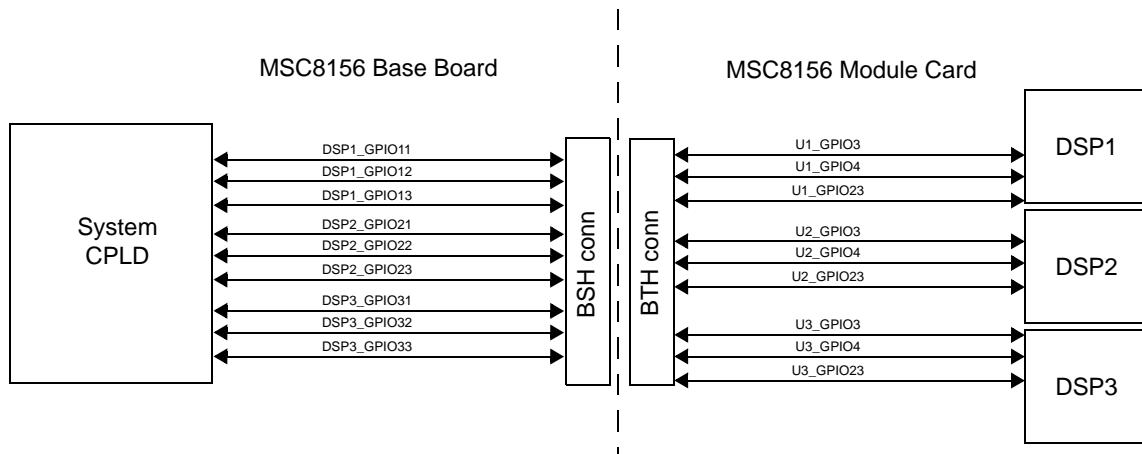


**Figure 0-7. JTAG/OnCE Connection**

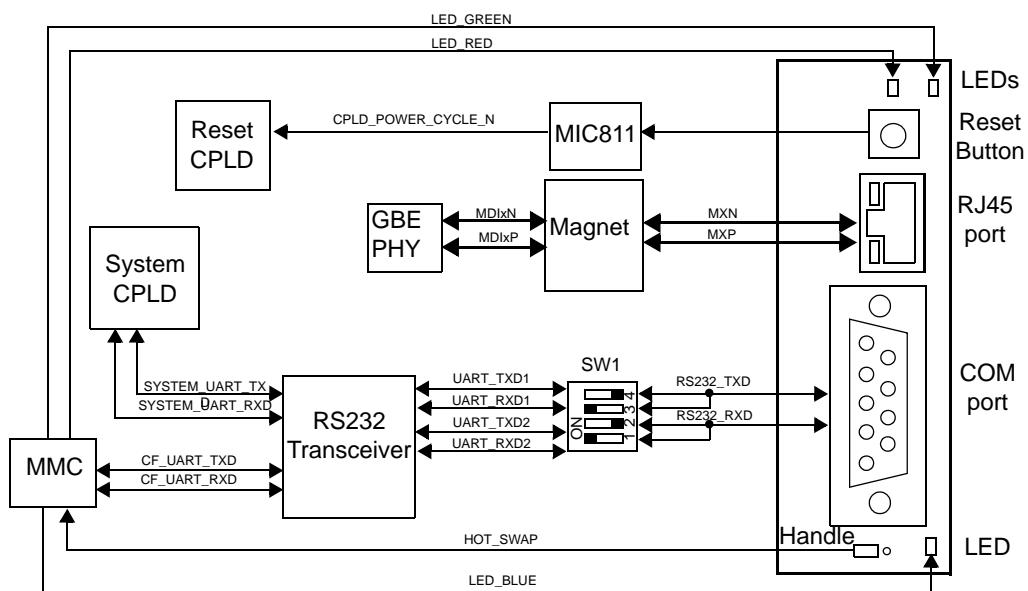
## 0.5.9 Interrupt



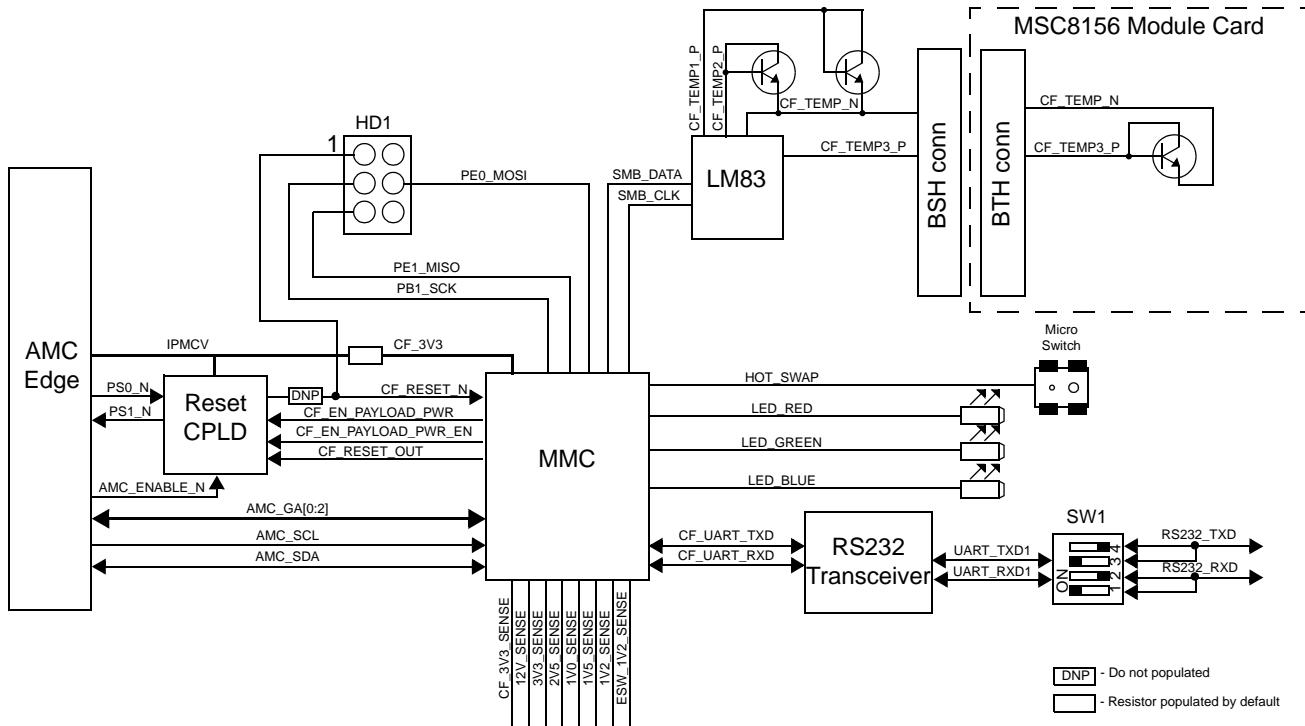
## 0.5.10 GPIOs



## 0.5.11 Front Panel



## 0.5.12 MMC



## 0.5.13 Power Supply and Budget

12V voltage will be provided by AMC connector.

DSP core voltage, DDR-III voltage, RGMII voltage, FPGA, switch/PHY specific voltages will be switching or linear regulated depending on the voltage drop and current consumption requirement.

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The table below summarizes the voltages on the MSC8156AMC.

**Table 0-2. Power Usage Summary (not updated...)**

Voltage	Usage	Budget	Solution
1V	VDD, AVDD1/2	<1A	MIC1510ETB+ regulator (3A) with tracking
1V	VDDC	10A?	MIC1953EUB+ switching
1.2V	VSC7385, 88E1111	1.75A + 0.4A	MIC37302 LDO (3A)
1.8V	DDR2	0.5A + DDR chip x2pcs	MIC37302 LDO (3A)

**Table 0-2. Power Usage Summary (not updated...)**

Voltage	Usage	Budget	Solution	
2.5V	RGMII	0.2A + 0.2A + 0.2A	MIC39100-2.5WS (1A)	
3.3V	General IO	Variable	Direct from ATX Power	
5V	Switching source	0.5-1A	Direct from ATX Power	
12V	None	None	Direct from ATX Power	

## 0.5.14 Module and Baseboard Connector Assignment

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## 0.5.15 Thermal Sim and Heatsink

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# 0.6 Resource Allocation (not updated...)

## 0.6.1 Reset Connection

## 0.6.2 GPIO Usage

The table below shows the GPIO usage on 8313-EVAL Board.

**Table 0-3. GPIO Usage**

Usage	Assignment	Pins Multiplexed
LCD connector GPIO[0-7]	GPIO[0-7]	LA[0-7]
LCD_EN	n/a, supported by LED/status reg	
SD Card CS#	GPIO13	LA8
DAC CS#	GPIO14	LA9
4 LEDs	n/a, supported by LED/status reg	
3-pin 1K EPROM	GPIO31	SPISEL#
SD_INSERT#	n/a, supported by LED/status reg	
SD_PROTECT	n/a, supported by LED/status reg	

Most of the other GPIOs are occupied by other functions such as I2C, TSEC pins, etc. For LEDs, SD card status, they will be supported by register built by buffer and latch on local bus.

## 0.6.3 Interrupt Usage

The table below shows the interrupt usage on 8313-EVAL Board.

**Table 0-4. Interrupt Usage**

Usage	Assignment	Pins Multiplexed
Not used	IRQ0#	
PCI slot INTA	IRQ1#	
PCI slot INTB, mini PCI INTA	IRQ2#	
88E1111 (OD), RTC (OD)	IRQ4#	
VSC7385, USB3300 supply (OD)	IRQ3#	
SD card SDIO mode	not supported	

OD means open drain.

## 0.6.4 Chip Select Usage

The table below shows the chip select usage on 8313-EVAL Board.

**Table 0-5. Chip Select Usage**

Usage	Assignment	Pins Multiplexed
NAND Flash	CS0# CS1# swappable	
NOR Flash	CS1# CS0# swappable	
VSC7385	CS2#	
LED, status register	CS3#	